ABSTRACT

A device that synchronizes circuits over asynchronous links is disclosed. Some embodiments of the invention include a device that comprises a plurality of circuits. One of the plurality of circuits is designated as a "master" circuit. The master circuit is configured to send a first synchronization signal to one or more of the plurality of circuits, and each circuit that receives the first synchronization signal is configured to responsively send a second synchronization signal to one or more of the plurality of circuits.